

Refine Search

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Terms	Documents
(709/253 345/520 345/531 710/100 710/33 710/300 710/301 710/302 710/72 710/306 710/313 326/37 361/679 361/683 361/783).ccls.	11664

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L1 710/100,33,300-
 302,72,306,313;345/520,531;361/679,683,783;709/253;326/37.ccls.

11664 L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L1 and L2	20

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<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L4</u> 11 and 12	20	<u>L4</u>
<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L3</u> (PCI adj1 Express) same port same (more or less or smaller or greater)	1	<u>L3</u>
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L2</u> (PCI adj1 Express) same port same (more or less or smaller or greater)	206	<u>L2</u>
<u>L1</u> 710/100,33,300-		
302,72,306,313;345/520,531;361/679,683,783;709/253;326/37.ccls.	11664	<u>L1</u>

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Freeform Search

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Term:	<div style="border: 1px solid black; padding: 2px;"> L15 and PCI <div style="float: right;"> <input type="button" value="▲"/> <input type="button" value="▼"/> </div> </div>
Display:	<div style="border: 1px solid black; padding: 2px; display: inline-block;">10</div> Documents in Display Format: <div style="border: 1px solid black; padding: 2px; display: inline-block;">-</div> Starting with Number <div style="border: 1px solid black; padding: 2px; display: inline-block;">1</div>
Generate: <input type="radio"/> Hit List <input checked="" type="radio"/> Hit Count <input type="radio"/> Side by Side <input type="radio"/> Image	

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side by side			
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>			
<u>L16</u>	L15 and PCI	7	<u>L16</u>
<u>L15</u>	port same connector same transmit\$4 same receiv\$3 same less	182	<u>L15</u>
<u>L14</u>	L13 same PCI	1	<u>L14</u>
<u>L13</u>	port same connector same transmit\$4 same less	336	<u>L13</u>
<u>L12</u>	L11 same PCI	6	<u>L12</u>
<u>L11</u>	port same connector same less	3770	<u>L11</u>
<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L10</u>	L9 and PCI	0	<u>L10</u>
<u>L9</u>	port same connector same less	85	<u>L9</u>
<u>L8</u>	PCI\$10 same port same connector same less	0	<u>L8</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L7</u>	PCI\$10 same port same connector same less	5	<u>L7</u>
<u>L6</u>	L5 same connector	3	<u>L6</u>
<u>L5</u>	"PCI-Express" same port same (more or less)	30	<u>L5</u>
<i>DB=USPT,PGPB; PLUR=YES; OP=OR</i>			

Refine Search

Search Results -

Terms	Documents
L20 and PCI	2

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<u>L22</u>	L20 and PCI	2	<u>L22</u>
<u>L21</u>	L20 same PCI	0	<u>L21</u>
<u>L20</u>	"first port connector" near5 (more or less) "second port connector"	75	<u>L20</u>
<u>L19</u>	L17 same PCI	14	<u>L19</u>
<u>L18</u>	L17 and PCI	89	<u>L18</u>
<u>L17</u>	port same transmit\$4 same receiv\$3 same connector same (more or less)	1243	<u>L17</u>
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>			
<u>L16</u>	L15 and PCI	7	<u>L16</u>
<u>L15</u>	port same connector same transmit\$4 same receiv\$3 same less	182	<u>L15</u>
<u>L14</u>	L13 same PCI	1	<u>L14</u>
<u>L13</u>	port same connector same transmit\$4 same less	336	<u>L13</u>
<u>L12</u>	L11 same PCI	6	<u>L12</u>
<u>L11</u>	port same connector same less	3770	<u>L11</u>

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L10 L9 and PCI 0 L10

L9 port same connector same less 85 L9

L8 PCI\$10 same port same connector same less 0 L8

DB=PGPB,USPT; PLUR=YES; OP=OR

L7 PCI\$10 same port same connector same less 5 L7

L6 L5 same connector 3 L6

L5 "PCI-Express" same port same (more or less) 30 L5

DB=USPT,PGPB; PLUR=YES; OP=OR

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'20030188076'| '20030202510')![pn] 14 L4

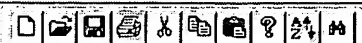
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[pn] 7 L3

DB=USPT; PLUR=YES; OP=OR

L2 6789154.uref. 2 L2

L1 6789154.pn. 1 L1

END OF SEARCH HISTORY



- Drafts
- Pending
- Active
 - L1: (15) (PCI adj1 Express
 - L2: (12) 11 same bus
- Failed
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- UDC
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DBs: USPAT

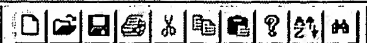
☒ Plurals

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11 same bus

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 7120722 B2	20061010	16	Using information provided through tag space	710/305	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 7111246 B2	20060919	19	User interface accorded to tiered object-related trust	715/809	715/738; 715/741;
3	<input type="checkbox"/>	<input type="checkbox"/>	US 7107384 B1	20060912	13	Dynamic PCI-bus pre-fetch with separate counters for	710/309	382/305; 710/314;
4	<input type="checkbox"/>	<input type="checkbox"/>	US 7103064 B2	20060905	35	Method and apparatus for shared I/O in a load/store	370/463	370/465
5	<input type="checkbox"/>	<input type="checkbox"/>	US 7096308 B2	20060822	19	LPC transaction bridging across a PCI.sub.--express	710/315	710/306
6	<input type="checkbox"/>	<input type="checkbox"/>	US 7096305 B2	20060822	29	Peripheral bus switch having virtual peripheral bus and	710/312	710/104
7	<input type="checkbox"/>	<input type="checkbox"/>	US 7075541 B2	20060711	17	Adaptive load balancing in a multi-processor graphics	345/505	345/502; 345/506;
8	<input type="checkbox"/>	<input type="checkbox"/>	US 7058738 B2	20060606	12	Configurable PCI express switch which allows multiple	710/104	370/389; 710/100;
9	<input type="checkbox"/>	<input type="checkbox"/>	US 7046668 B2	20060516	35	Method and apparatus for shared I/O in a load/store	370/392	370/401; 709/249
10	<input type="checkbox"/>	<input type="checkbox"/>	US 7043667 B2	20060509	13	Debug information provided through tag space	714/43	
11	<input type="checkbox"/>	<input type="checkbox"/>	US 7024510 B2	20060404	11	Supporting a host-to-input/output (I/O)	710/311	710/312



- Drafts
- Pending
- **Active**
 - L1: (15) (PCI adj1 Express
 - L2: (12) 11 same bus
- Failed
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- UDC
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 DBs: ☒ PluralsDefault operator: ☒ Highlight all hit terms initially

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	15	(PCI adj1 Express) same port same (more or less or	USPAT	2006/10/30 16:24			
2	BRS	L2	12	11 same bus	USPAT	2006/10/30 16:24			


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» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ **1. Performance evaluation of InfiniBand with PCI Express**
Jiuxing Liu; Mamidala, A.; Vishnu, A.; Panda, D.K.;
[High Performance Interconnects, 2004. Proceedings. 12th Annual IEEE Symp.](#)
25-27 Aug. 2004 Page(s):13 - 19
Digital Object Identifier 10.1109/CONNECT.2004.1375193
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- ☐ **2. Options for high-volume test of multi-Gb/s ports**
Johnson, J.C.;
[Test Conference, 2004. Proceedings. ITC 2004. International](#)
2004 Page(s):1435
Digital Object Identifier 10.1109/TEST.2004.1387443
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- ☐ **3. HARTIK 3.0: a portable system for developing real-time applications**
Lamastra, G.; Lipari, G.; Buttazzo, G.; Casile, A.; Conticelli, F.;
[Proceedings - Fourth International Workshop on Real-Time Computing System](#)
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27-29 Oct. 1997 Page(s):43 - 50
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Performance evaluation of InfiniBand with PCI Express

Jiuxing Liu Mamidala, A. Vishnu, A. Panda, D.K.
Dept. of Comput. & Sci. & Eng., Ohio State Univ., Columbus, OH, USA

This paper appears in: [High Performance Interconnects, 2004. Proceedings. 12th Annual IEEE Symposium on](#)

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Posted online: 2005-01-03 08:24:28.0

Abstract

We present an initial performance evaluation of InfiniBand HCAs (host channel adapters) from Mellanox with PCI Express interfaces. We compare the performance with HCAs using PCI-X interfaces. Our results show that InfiniBand HCAs with PCI Express can achieve significant performance benefits. Compared with HCAs using 64 bit/133 MHz PCI-X interfaces, they can achieve 20%-30% lower latency for small messages. The small message latency achieved with PCI Express is around 3.8 /spl mu/s, compared with the 5.0 /spl mu/s with PCI-X. For large messages, HCAs with PCI Express using a single port can deliver unidirectional bandwidth up to 968 MB/s and bidirectional bandwidth up to 1916 MB/s, which are, respectively, 1.24 and 2.02 times the peak bandwidths achieved by HCAs with PCI-X. When both the ports of the HCAs are activated, HCAs with PCI Express can deliver a peak unidirectional bandwidth of 1486 MB/s and aggregate bidirectional bandwidth up to 2729 MB/s, which are 1.93 and 2.88 times the peak bandwidths obtained using HCAs with PCI-X. PCI Express also improves performance at the MPI level. A latency of 4.6 /spl mu/s with PCI Express is achieved for small messages. And for large messages, unidirectional bandwidth of 1497 MB/s and bidirectional bandwidth of 2724 MB/s are observed.

Index Terms
Inspe

Controlled Indexing

[peripheral interfaces](#) [system buses](#)

Non-controlled Indexing

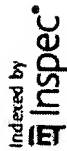
133 MHz 1486 MB/s 1497 MB/s 2724 MB/s 4.6 mus 64 bit I/O bus Mellanox
InfiniBand host channel adapters **PCI Express** interfaces **PCI-X** interfaces **Peripheral**
Component Interconnect **bidirectional bandwidth** **small message latency** **unidirectional**
bandwidth

Author Keywords
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References
No references available on IEEE Xplore.

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